II. Latch-up Prevention

The probability of inducing and maintaining latch-up is greatly reduced by the epitaxial layer/low-resistance substrate fabrication process used for SVX4. Theoretically, latch-up could still occur if transient voltages in excess of (xVDD + 0.3 v) or (xGND – 0.3 v) are applied to I/O pins. Such conditions could also initiate conduction of the ESD protection diodes, which could be damaged. It should be stressed that these classic latch-up trigger mechanisms, as depicted in Figure 1, are very unlikely to occur due to the low Rpsub. It would take much more than 200 mA to induce latch-up of the NMOS devices because of the low substrate resistance. This current compliance value meets the generally accepted requirement for latch-up immunity on I/O pins. A more serious mechanism that could lead to DVDD latch-up is described below.

There are five separate power busses on SVX4_V1 and three on SVX4_V2. In either case, all busses are connected to one of two supplies off-chip, AVDD/AGND or DVDD/DGND. The impedance between DGND and AGND should be kept low in order to prevent a potential difference developing between DGND and AGND (Vad in Figure 2b) of more than 0.3 v, which could induce latch-up of the digital section. Such conditions could also initiate conduction of the ESD protection diodes, which could be damaged. This potential latch-up mechanism is depicted in Figure 2a below. In this case the low substrate resistance is not a factor in killing the forward bias on the parasitic NPN, which is instead dependent on external impedances. Furthermore, the typical NWELL resistance remains relatively high compared to the substrate resistance, creating the possibility for latch-up to be induced. Should this situation occur, the resulting large current conducted through $Z_{hybid+bond}$ would likely kill the forward bias at the parasitic NPN emitter. In any event, it is recommended that the AVDD power supply be energized before DVDD in order to avoid a transient condition that might violate the above requirement.

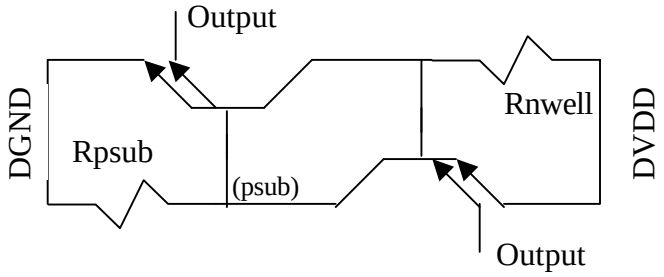

Figure 1: Classic parasitic bipolar latch-up circuit.

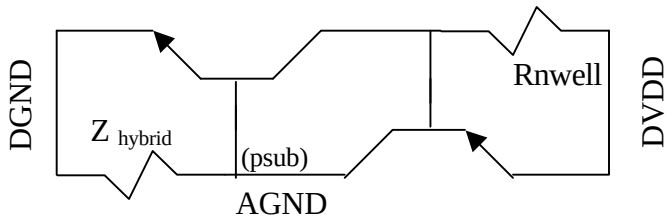

Figure 2a: Dual-supply latch-up mechanism

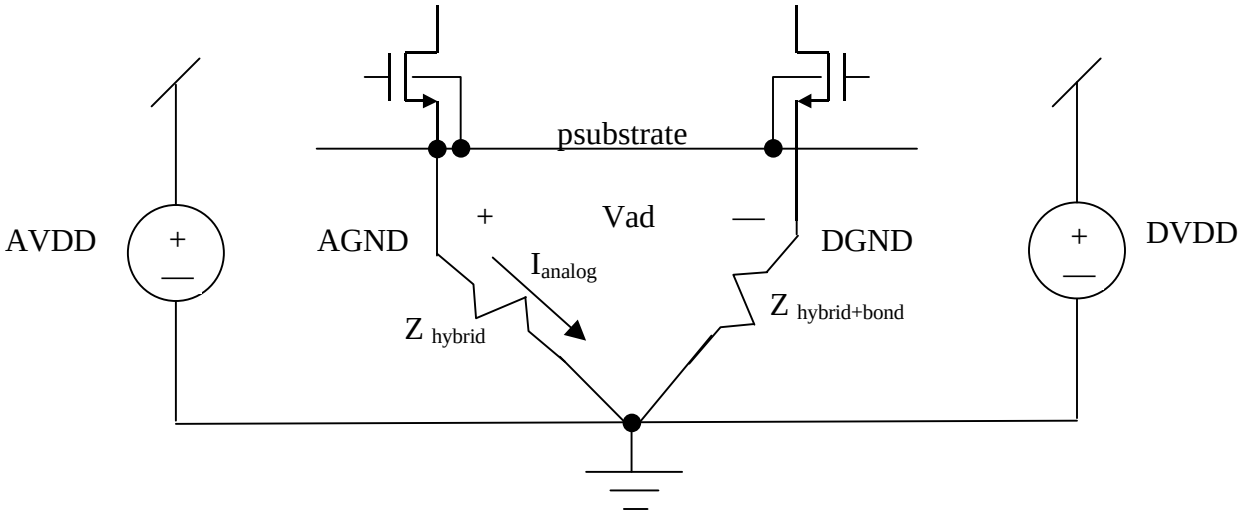

Figure 2b: Equivalent circuit.